(54) METHOD FOR FORMING SOLDER BUMP
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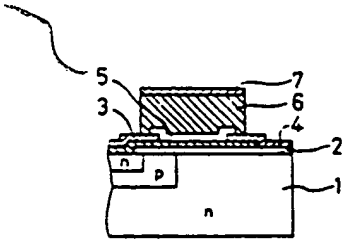
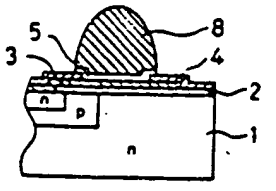
PURPOSE: To form a solder bump which is characterized by the features that a photoresist is readily removed and damages are not remained in characteristic checking, by melting a solder-plated layer at a specified temperature and curing it, thereafter melting the solder layer at a higher temperature and curing it again.

CONSTITUTION: A surface-protecting film 4 is further deposited on an Al wiring 3 which contacts with Si and the window portion of a surface-protecting film 2 on a Si substrate 1, and an underlying metal layer 5 is formed at said window portion. Thereafter, a Pb layer 6 and an Sn layer 7 are stacked by electric plating with a photoresist being a mask. Then, the plated layers 6 and 7 are melted at a temperature less than 320°C, and the photoresist is removed after said layers have been cooled and cured. At this stage, the characteristic check of the element is performed. Thereafter, the temperature is increased again, and the soldering layers are melted again at a temperature higher than the previous melting temperature (e.g., 330~350°C for the solder comprising 90% of Pb and 10% of Sn), thereby a semi-circular solder bump 8 is obtained. In this constitution, even though damages are given in the characteristic check, the remnants of the damages are not remained.





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㊹はんだバンプ形成方法

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明　細　書

1. 発明の名称　はんだバンプ形成方法

2. 特許請求の範囲

1) はんだめっき層を 320℃ 以下の温度において融解して溶固させた後さらに高い温度で再融解して溶固させることを特徴とするはんだバンプ形成方法。

3. 発明の詳細な説明

本発明はフリップチップ素子などのボンディングのための電極と接続されるはんだバンプの形成方法に関する。

このようなはんだバンプを選択蒸着により形成することはバンプ高さの制御が困難で処理コストが高い欠点があるので、通常ははんだめっきを利用して行われる。第 1 図に示すようにフリップチップ素子においてはシリコン基板 1 の上に設けた、例えば酸化シリコンから成る表面保護膜 2 の窓部でシリコンと接触するアルミニウム配線 3 の上にさらに、例えば窒化シリコン膜から成る表面保護膜 4 を設け、その窓部に、例えば Ti, Cu, Ni の 3 層を順次蒸着して形成する下地金属層 5 を設ける。この下地金属層 5 の上にホトレジストをマスクとして Pb 層 6 および Sn 層 7 を電気めっきにより積層する。次いでこの Pb 層および Sn 層を 340 − 350℃ の温度で融解して合金させ、第 2 図に図示するような半球状のバンプ 8 に成形する。(第 2 図の第 1 図と同一の部分には同じ符号が付してある。) 第 1 図において Pb 層の厚さを約 80 μm、Sn 層の厚さを約 10μm にすれば、バンプの合金は重量比で Pb 90%、Sn 10% のはんだとなり、バンプの高さは約 100μm となる。はんだバンプの周囲に設置したホトレジストは、はんだバンプの成長後に除去すると除去用の有機系の酸がめっき層を腐食するのでこの融解工程の後で除去される。さらにはんだに覆われていない下地金属層を除去し、素子の特性チェックを行う。しかし上述の工程においては素子の特性チェックの際にバンプが損傷を受けやすい。またはんだ融解時にホトレジストが焼付いてその除去が不完全になることがある。

本発明の目的は上述の方法と異なり、ホトレジ

(1)　　(2)

ストの除去が容易でしかも特性チェックの際の損傷を受けないはんだバンプの形成方法を提供することにある。

この目的を達成するために本発明に基づく形成方法は次のような工程をとる。すなわち第1図に示すようなはんだめっきを施した後320℃以下の温度でめっき膜を熱処理し、冷却後溶剤でホトレジストを除去する。この温度ではレジストは変質せず、焼付くことがないので除去は容易である。そしてこの段階で素子の特性チェックを行う。この後再び温度を上げて前の熱処理温度より高い温度、例えばPb90%、Sn10%のはんだでは330～350℃ではんだ層を再熱処理して第2図のような半球状の良い外形状を得る。この再熱処理により特性チェックの際に損傷を受けてもその損傷が残ることはなく、以後の特性に支障を来たすことがない。最後にはんだで覆われない下地金属層をエッチングで除去した素子は組立工程に付される。

上述の例では、はんだめっき層はSnめっきとPbめっきの2層として形成されるが、1層の合金めっきにより形成されたはんだめっき層に対しても本発明は適用できる。

以上のように本発明によるバンプの形成方法は、はんだめっき層の熱処理を2工程に分けることにより、その中間にホトレジストの除去や特性チェックの工程等を介在させることができ、得られたバンプが特性的にも外観的にも支障のないものにすることを可能にする。

4図面の簡単な説明

第1図は本発明の適用される例であるフリップチップ素子の一部分のはんだめっき後の断面図、第2図は同じくはんだバンプ形成後の断面図である。

6—Pbめっき層、7—Snめっき層、8—はんだバンプ。

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Fig. 1

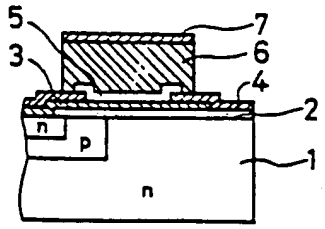
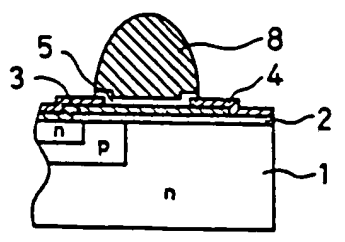


Fig. 2



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(54) METHOD OF BUILDING SOLDER BUMPS

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S P E C I F I C A T I O N S

1. Patent Name:

Method of Building Solder Bumps

2. Field of Patent Application:

A method of building solder bumps by which the solder-plated

layer is first dissolved at a temperature lower than 320°C, then cured, and after that dissolved again at a higher temperature and cured again.

3. Detailed Description

The invention is related to the electroplating method of forming solder bumps, which are used to bring flip-chip elements together.

In general, a weak point of the bumps applied for this purpose so far was the difficulty of controling the bump height, which consequently increased the processing costs. A solder plating method usually used in bump building is demonstrated in Fig. 1. The elements usually comprising a flip chip are mounted on silicon substrate material (1). The surface-protecting film (2), made of silicon oxide, is covered by aluminum wiring (3). The silicon and the aluminum wiring come into contact at the window section where the surface-protecting film (2) does not cover the silicon substrate. The aluminum wiring is covered by the surface-protecting film made of silicon-(?) film (4), and the window inside the silicon-(?) film (4) is covered by under-bump metallurgy (5) which is composed of three successively deposited layers of Ti, Cu, and Ni. This under-bump metallurgy (5) is masked with a photoresist, and a layer of Pb (6) and a layer of Sn (7) which are laminated by electroplating. Then, the layer of Pb and the layer of Sn are dissolved at a temperature between 340 - 350°C making an alloy. As the result, a semispheric bump (8) is formed, as shown in Fig. 2. (The same numbers are attached to corresponding elements in Fig. 1

and Fig. 2.) If the thickness of Pb layer shown in Fig. 1 is about 50 μm, and if the thickness of Sn layer is about 10 μm, then Pb will make up 90% of the bump-alloy relative weight, and Sn will make up the remaining 10%. The height of the bump will be approximately 100 μm. If the photoresist deposited during the solder plating is removed immediately after the solder plating, the organic acid used for removal will erode the plated layer. For this reason, the photoresist is removed after the dissolving process. After removing the under-bump-metallurgy layer which is not covered by the solder plate, the specific check of the elements is carried out. However, the bumps can easily be damaged when the specific check of elements is carried out. Also, in some cases the photoresist may sinter during the dissolving process, and after that its removal will be incomplete.

The objective of this invention is to produce a result different from the results of the processing described above. This method of solder-bump building provides an easy removal of photoresists and protects from damage during the specific check.

In order to accomplish the objective, this invention introduces a building method as described hereafter. After the solder plating shown in Fig. 1 has been completed, the plated layer is dissolved at a temperature lower than 320°C, and after the cooling and curing the photoresist is removed. The resist does not deteriorate at this temperature, and it can be easily removed because there is no sintering. At this point the specific check is carried out. Then, the temperature is raised above the previous

dissolving temperature which was between 330-350°C for the solder comprised of 90% of Pb and 10% of Sn. Then, the solder layer is dissolved again to build up the final semispheric form, as shown in Fig. 2. Even if a damage occurs when the specific check is carried out, the repeated dissolving process makes sure that the damage does not remain and does not cause problems afterwards. Finally, the under-bump-metallurgy layer which had not been covered by solder is removed by etching, and the flip-chip elements are assembled.

In the above described example, the solder plating was comprised of two layers, the plated Sn and the plated Pb. This invention can also be applied, however, in the solder plating comprised of only one layer of plated alloy.

In summary, this method of building solder bumps divides the dissolving the solder-plated layer into two steps and enables the photoresist removal and the specific check to be carried out between the two steps. The characteristics and the external appearance of the bumps obtained by this method are free of defects.

4. Simple Description of Figures

Fig. 1 shows the cross-sectional view of an application of this invention after the flip-chip elements had been partly solder plated. Fig. 2 shows the same example after the bump form had been built.

6 ... Pb-Plated Layer

7 ... Sn-Plated Layer

8 ... Solder Bump

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